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| EXAMINER | |
|---|---|
| PAN, DANIEL H | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/836,541 | KINTER ET AL. | |
| | Examiner | Art Unit | |
| | Daniel Pan | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3,5,6,8 and 10-20* is/are pending in the application.

4a) Of the above claim(s) *4,7 and 9* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,8 and 10-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 August 2001* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/20/05,09/28/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-3,5,6, 8, 10-20 are presented for examination. Claims 4, 7, 9 have been canceled.

2. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn. In view of the pre-appeal conference, the final action on 11/28/05 has been withdrawn. This is a non-final action and includes new ground of rejections .

In view of the Pre-Appeal Conference Request filed on 04/27/06, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 5,10, 13,14,15,17-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The reasons are given below.

4. As to claim 5, no physical transformation can be found in the claim . Although claim recites a cache controller for decoding and execution by the processor, no details of decoding and execution can be found in the claim, and it is an intended use, and not a positive claim limitations. What is selected is neither applied in a disclosed practical application nor made available for use in a disclosed practical application. Instead, it appears to be nothing more than an idea. The reading , mapping , and selective steps present no substantial practical application.

As to claim 10, Claim 10 additionally recites the tangible computer readable medium in preamble. However, in view of the specification, there is no clear definition that the computer readable medium is necessary a hardware. Page 13, [0054] of the specification taught computer usable (e.g. readable ) medium include both hardware , CD ROM, DVD ROM and not hardware as a computer data signal embodied in computer usable transmission medium (e.g. carrier wave). Therefore, it is not necessarily implemented in hardware. A tangible medium absent a dictionary definition

is a medium capable of being perceived. Signals are capable of being received therefore it is directed to 101 problem. An amendments to the claim and specification should clarify medium issue of 101 and would not introduce new matter as the addition of a group label doesn't change the scope of the disclosure .

If selecting were just determining which signal to output then selection would not be a tangible result. Applicant is suggested to clarify that the final result were the selection of an input signal using a selector signal by the multiplexer and achieving practical application.

Although claim recites a cache controller for decoding and execution by the processor, no details of decoding and execution can be found in the claim, and it is an intended use, and not a positive claim limitations.

5. As to claims 13,14, claim 13,14 add no substantial practical application to parent claim 10 , and the Verilog hardware description language software is not tangible.

6. As to claims 15,20, see discussion on claim 10. The transmission of the computer readable program code is not tangible.

7. As to claims 17,18,19, claim 17,18, 19 add no substantial practical application to parent claim 10, and the Verilog hardware description language software is not tangible.

8. As to claim 8, after a further review, claim 8 is not being rejected under "101" because it shows the processor's functional units, such as the execution unit, the decoder and the cache for storing the instructions and the parallel performance of the

mappers. However, examiner would like to suggest a clear recitation of the structural relation among the execution unit , decoder, and the instruction cache to avoid a likely broader interpretation of the claim language. A structural relation, such as an input and output connection, could show a physical transformation.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-3,5,6,8,10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brennan (5,740,392) in view of Lee (6,442,674).

10. As to claim 1, Brennan taught a cache controller for use with a processor, comprising:

A) a plurality of mappers (see length decoders 35 in fig.5) for receiving instructions of an instruction set, each mapper for mapping an instruction of said instruction set to a predetermined instruction width format IPIWFI configuration (see length 00H and 0FH), wherein the plurality of mappers include at least one first mapper and at least one second mapper for receiving instructions from an instruction cache (see instruction cache 30 to the decoders 35 in fig.4); and

b) a multiplexor (see mux) for mappers and selecting, in response to a selector signal, a desired one of said PIWF configurations for decoding and execution by the processor.

receiving the PIWF configurations from the plurality of mappers (decoders) and selecting in response to a select signal [select] a desired one of the configurations (see also the length decoders 40 in 35 in col.6, lines 66-67, col.7, lines 1-49, see also a plurality of parallel decoders in fig.8, see the shifter 38 used as a mux in col.6, lines 40-52).

11. Brennan did not specifically show his mappers receiving instructions from a fill buffer as claimed . However, Lee taught a fill buffer (see fig.1 [100], col.2, lines 19-53). It would have been obvious to one of ordinary skill in the art to use Lee in Brennan for including the fill buffer as claimed because the use of Lee could provide Brennan the ability to accept instructions from different source (e.g. a buffer, or the like), therefore enhance the adaptability of Brennan, and because Brennan also taught receiving instructions from a cache (see fig.4 [instruction cache 30]), which was recognizable by one of ordinary skill in the art that the cache had been known to be an alternative memory resource of the main memory for providing a faster access, and any smaller storage, such as a buffer, or the like, would have been provided in the system to increase the read/write speed of the instructions, and in doing so, provided a motivation.

12. As to Claim 2, a tag comparison (see detection on most significant bits with the 0FH in col.6, lines 40-52) for the selector signal [select].

13. As to claim 3, comparing, for each instruction provided to one of the plurality of

mappers, a tag (see most significant bits 0-2) associated with an instruction of the instruction set to a desired tag (0FH) and generating the selector signal (select) to cause said multiplexor to select said desired one of said PIWF configurations.

14. As to claim 5, Brennan also (a) reading instructions of the instruction set from an instruction cache into a plurality of mappers (see fig.5 decoders) , wherein at least one of the instructions was read from the instruction cache and at least one of said instructions is read from the buffer, each instruction of the instruction set being read into a corresponding one of the plurality of mappers in preparation for mapping (see instruction cache 30 to the decoders 35 in fig.4);

(b) mapping each instruction of said instruction set to a corresponding PTWF configuration (see length 00H and 0FH); and

(c) selecting a desired one of said PIWF configurations for decoding and execution by the processor (see also the length decoders 40 in 35 in col.6, lines 66-67, col.7, lines 1-49, see also a plurality of parallel decoders in fig.8, see the shifter 38 used as a mux in col.6, lines 40-52).

Brennan did not specifically show his mappers receiving instructions from a fill buffer as claimed . However, Lee taught a fill buffer (see fig.1 [100], col.2, lines 19-53). The reasons of obviousness were already given in paragraph 15. Therefore, it will not be repeated herein.

15. As to claim 6, Brennan also included comparing, for each instruction provided to one of said plurality of mappers, a tag 9most significant bit) associated with an instruction of the instruction set to a desired tag (0FH) , wherein the desired one of the PIWF configurations is selected based on the comparison or detection (see the selection).

16. As to claim 8, Brennan also included at least :

a) decoder (see either fig.4 instruction decoder or decoder 35 ),

b) cache for storing instructions (see cache 30 in fig.4); and

c) a cache controller (not explicitly characterized, but see how the prefetch of instructions from the cache 30 in fig.4) for retrieving the instructions from the cache and providing the instructions to a decoder (see fig.4 35, see fig.5 for details of the decoder 35), comprising:

a plurality of mappers for mapping a plurality of instructions of an instruction set to predetermined instruction width format (PIWF) configurations (see 0FH 00H), the plurality of mappers including at least one first mapper for receiving instructions and at least one second mapper for receiving instructions from said instruction cache (see fig.4 instruction cache) ,

d) a multiplexor for selecting, in response to a selector signal, one of said PIWF configurations for decoding by the decoder (see col.6, lines 40-52) and execution by said execution unit,

e) means for comparing, for each instruction provided to the multiplexor, a tag (see most significant bits) associated with an instruction of the instruction set to a desired tag (0FH) and generating the selector signal to cause said multiplexor to select said desired one of the configurations (see col.6, lines 40-52) , whereby performing instruction mapping substantially in parallel with tag comparison to improve processor performance (see parallel decoders as mappers in fig.5 and fig.8). Brennan did not specifically show his mappers receiving instructions from a fill buffer as claimed . However, Lee taught a fill buffer (see fig.1 [100], col.2, lines 19-53). The reasons of obviousness were already given in paragraph 15. Therefore, it will not be repeated herein.

17. As to claim 10 , claim 10 is substantially the same as claim 1, and rejected under the same reasons as applied to claim 1. claim 10 additionally recites the microprocessor core embodied in software. Examiner holds that a microprocessor embodied in software is well known art (see the pertinent reference Palnitkar et al. 5,539,680., col.1, lines 15-22, cited in this action in paragraph, Palnitkar is not being used but it is ready to show examiner's position of well known art ).

18. As to claim 11 , see the selection in col.6, lines 40-52.

19. As to claim 12 , also included a microprocessor core is embodied in hardware description language software (see the pertinent reference Palnitkar et al. 5,539,680, col.1, lines 15-22 , cited in this action in paragraph, Palnitkar is not being used but it is ready to show examiner's position of well known art ).

20. As to claim 13,14, examiner holds that microprocessor core embodied in Verilog hardware description language software or VHDL had been known in the art (see the pertinent reference Palnitkar et al. 5,539,680, col.1, lines 15-22 , cited in this action in paragraph, Palnitkar is not being used but it is ready to show examiner's position of well known art ).

21. Claims 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brennan (5,740,392) in view of Lee (6,442,674) in view of Chang et al. (Design A Java Microprocessor Core Using FPGA Technology, IEEE 1998)

22. As to claim 15, claim 15 is substantially the same as claim 1, therefore rejected under the same reasons as set forth in the paragraph 15 above. Claim 15 additionally recites transmitting the microprocessor core over a communications network. Neither Brennan nor Lee specifically show the transmission of microprocessor core as claimed. However, Chang disclosed a microprocessor core (see the design of the Java microprocessor soft core in the introduction in page 13). It would have been obvious to one of ordinary skill in the art to use Chang in Brennan for transmission of the microprocessor core as claimed because the use of Chang could provide Brennan the

capability to expand the microprocessor functionalities into a network system, and because Chan also concluded that the Java could be distributed in client and server environment (see page 17), therefore it could be recognized by one of ordinary skill in the art that Chang's microprocessor core (see the Java soft core) could be transmitted in a network, such as client and server environment, and since no specific transmission details can be found in the claim body, it is read as a transmission in general, and therefore, examiner holds that transmission in general should also be applicable in Brennan's general purpose microprocessor (see Intel microprocessor in col.1, lines 32036) in order to enhance the interface connection of the system, for the above reasons, provided a motivation.

23. As to claim 16, Brennan also taught comparing, for each instruction provided to one of the plurality of mappers, a tag (see most significant bits 0-2) associated with an instruction of the instruction set to a desired tag (0FH) and generating the selector signal (select) to cause said multiplexor to select said desired one of said PIWF configurations.

24. As to claims 17, 18,19, examiner holds that microprocessor core embodied in Verilog hardware description language software or VHDL had been known in the art (see the pertinent reference Palnitkar et al. 5,539,680, col.1, lines 15-22 , cited in this

action in paragraph, Palnitkar is not being used but it is ready to show examiner's position of well known art ).

25. As to the internet in claim 20, see Chang's client and server environment in page 17.

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Wu et al. 2002/0107678 A1, paragraph [39] [49] is cited for the teaching of microprocessor implemented in hardware description language.

b) Palnitkar et al. 5,539,680, col.1, lines 15-22 , is cited for the teaching of the hardware description language.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

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*21 Century Strategic Plan*

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